|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  | 0 | 1 | 1 | 1 |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  | \* | 1 | 0 | 1 | 0 |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  | 0 | 0 | 0 | 0 |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  | 0 | 1 | 1 | 1 |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  | 0 | 0 | 0 | 0 |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  | 0 | 1 | 1 | 1 |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  | 1 | 0 | 0 | 0 | 1 | 1 | 0 |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

Shift reg

Adder

B

A

Combined Multiplier/Divider:

Clock/Control

16-bit abs value

Multiplicand/divisor

16-bit abs value

Multiplier/dividend

Cout 16-bit CLA Cin

33-bit shift register (left and right shifting)

32-bit negator